

FIG. 1

The diagram illustrates a memory subsystem architecture. On the left, a **Processor 202** is connected to a **Memory Controller 212** via a bidirectional bus **206**. The Memory Controller 212 is part of a **Flash Memory Subsystem 204**. A vertical bus **236** connects the Memory Controller 212 to multiple **Flash Memory Devices 214**. Each device contains a **Flash Memory Cell Array 216**. The subsystem 204 also includes a **Flash Memory Device 214** at the bottom, indicated by a vertical ellipsis. The processor 202 is also connected to the subsystem 204 via a bidirectional bus **208** and a unidirectional bus **210**.

FIG. 2

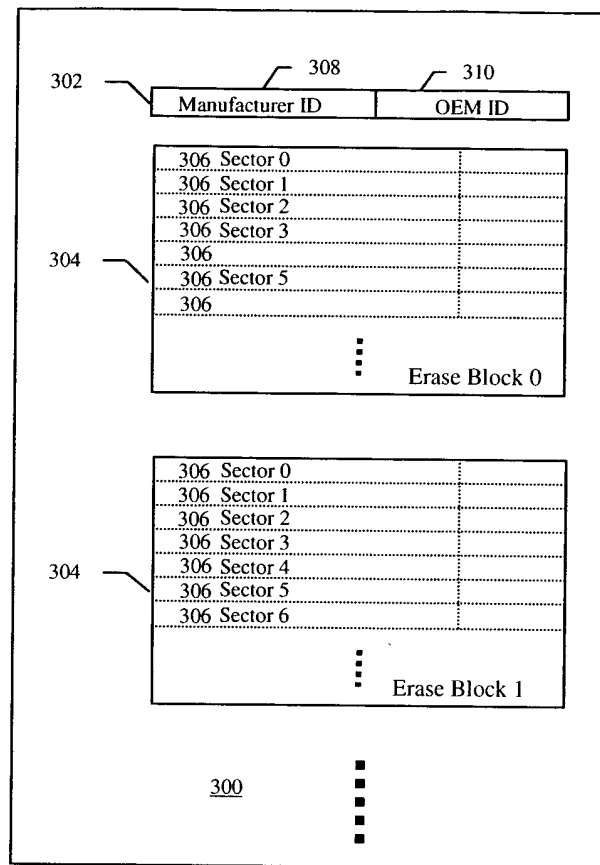


FIG. 3A

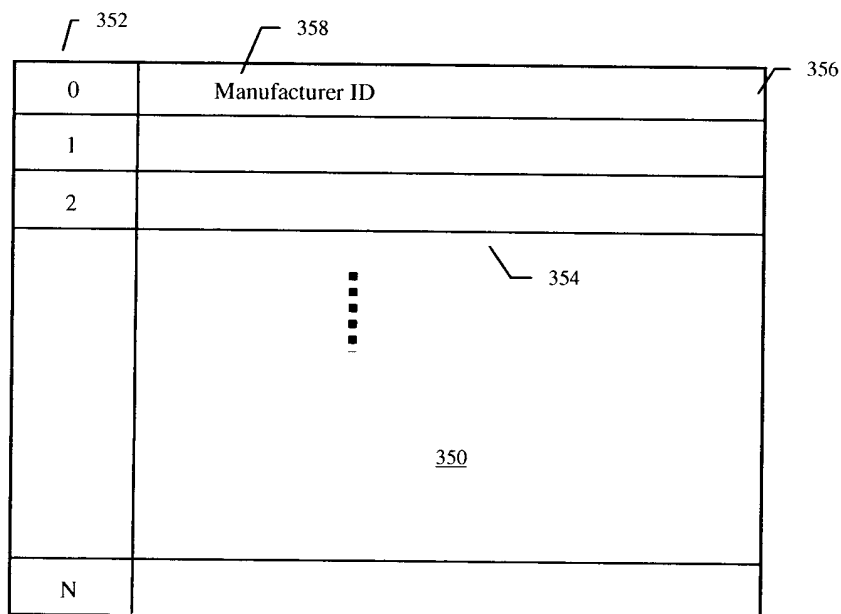


FIG. 3B

400

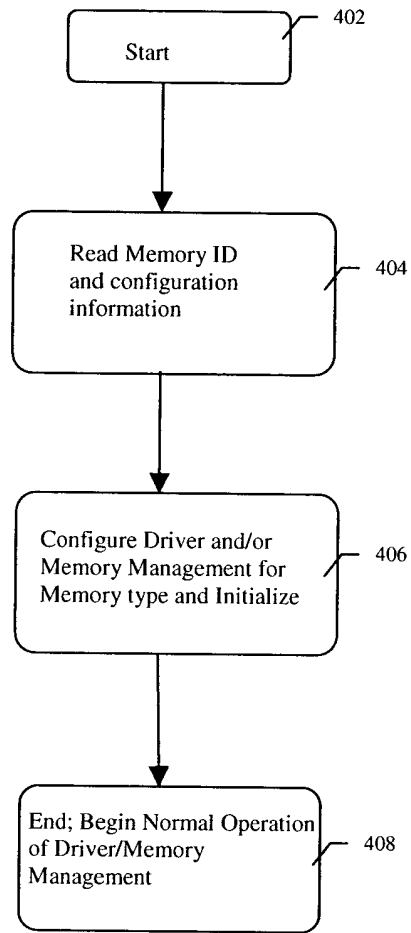


FIG. 4